MM 433 Manufacturing Process Seminar

Manufacturing of Transistors

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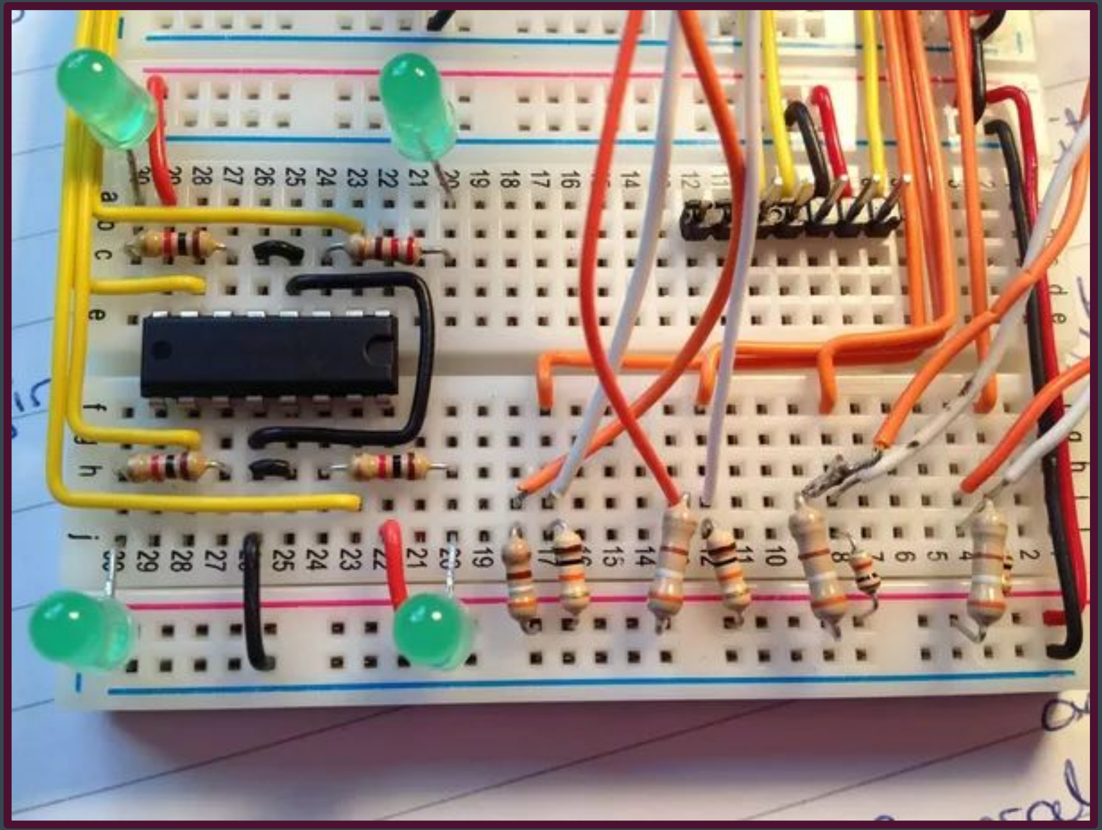
Outline

Intro to Transistor technology- Kedar

Fabrication and Developments- Som

Market Analysis and Future- Onas

Discrete Circuit



Integrated circuit

There's Plenty of Room at the Bottom

Richard P. Feynman

I imagine experimental physicists must often look with envy at men like Kamerlingh Onnes, who discovered a field like low temperature, which seems to be bottomless and in which one can go down and down. Such a man is then a leader and has some temporary monopoly in a scientific adventure. Percy Bridgman, in designing a way to obtain-higher pressures, opened up another new field and was able to move into it and to lead us all along. The development of ever higher vacuum was a continuing development of the same kind.

I would like to describe a field, in which little has been done, but in which an enormous amount can be done in principle. This field is not quite the same as the others in that it will not tell us much of fundamental physics (in the sense of, "What are the strange particles?") but it is more like solid-state physics in the sense that it might tell us much of great interest about the strange phenomena that occur in complex situations. Furthermore, a point that is most important is that it would have an enormous number of technical applications.

What I want to talk about is the problem of manipulating and controlling things on a small scale.

As soon as I mention this, people tell me about miniaturization, and how far it has progressed today. They tell me about electric motors that are the size of the nail on your small finger. And there is a device on the market, they tell me, by which you can write the Lord's Prayer on the head of a pin. But that's nothing; that's the most primitive, halting step in the direction I intend to discuss. It is a staggeringly small world that is below. In the year 2000, when they look back at this age, they will wonder why it was not until the year 1960 that anybody began seriously to move in this direction.

Why cannot we write the entire 24 volumes of the Encyclopaedia Britannica on the head of a pin?

Let's see what would be involved. The head of a pin is a sixteenth of an inch across. If you magnify it by 25 000 diameters, the area of the head of the pin is then equal to the area of all the pages of the Encyclopaedia Britannica. Therefore, all it is necessary to do is to reduce in size all the writing in the Encyclopaedia by 25 000 times. Is that possible? The resolving power of the eye is about 1/120 of an inch—that is roughly the diameter of one of the little dots on the fine half-tone reproductions in the Encyclopaedia. This, when you demagnify it by 25 000 times, is still 80 angstroms in diameter—32 atoms across, in an ordinary metal. In other words, one of those dots still would contain in its area 1000 atoms. So, each dot can easily be adjusted in size as required by the photoengraving, and there is no question that there is enough room on the head of a pin to put all of the Encyclopaedia Britannica.

Furthermore, it can be read if it is so written. Let's imagine that it is written in raised letters of metal; that is, where the black is in the Encyclopaedia, we have raised letters of metal that are actually 1/25 000 of their ordinary size. How would we read it?

If we had something written in such a way, we could read it using techniques in common use today. (They will undoubtedly find a better way when we do actually have it written, but to make my point conservatively I shall just take techniques we know today.) We would press the metal into a plastic material and make a mold of it, then peel the plastic off very carefully, evaporate silica into the plastic to get a very thin film, then shadow it by evaporating gold at an angle against the silica so that all the little letters will appear clearly, dissolve the plastic away from the silica film, and then look through it with an electron microscope!

There is no question that if the thing were reduced by 25 000 times in the form of raised letters on the pin, it would be easy for us to read it today. Furthermore, there is no question that we would find it easy to make copies of the master; we would just need to press the same metal plate again into plastic and we would have another copy.

How Do We Write Small?

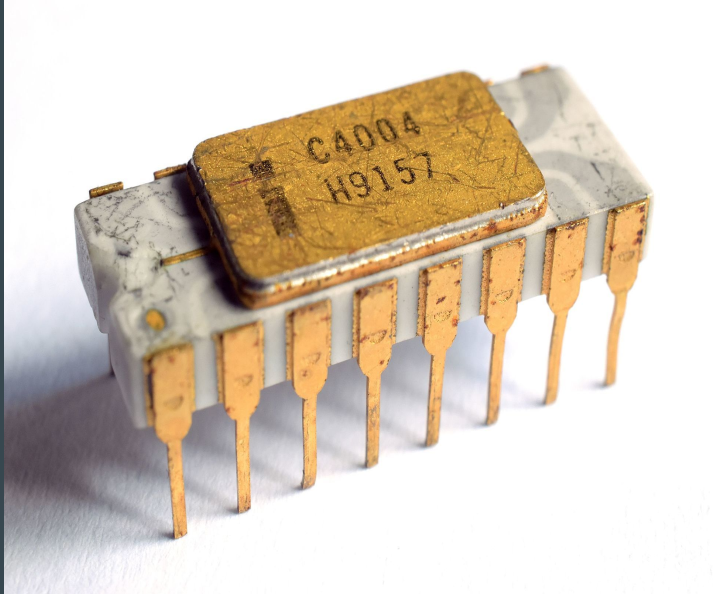
The next question is: How do we *write* it? We have no standard technique to do this now. But let me argue that it is not as difficult as it first appears to be. We can reverse the lenses of the electron microscope in order to demagnify as well as magnify. A source of ions, sent through the microscope lenses in reverse, could be focused to a very small spot. We could write with that spot like we write in a TV cathode ray oscilloscope, by going across in lines, and having an adjustment which determines the amount of material which is going to be deposited as we scan in lines.

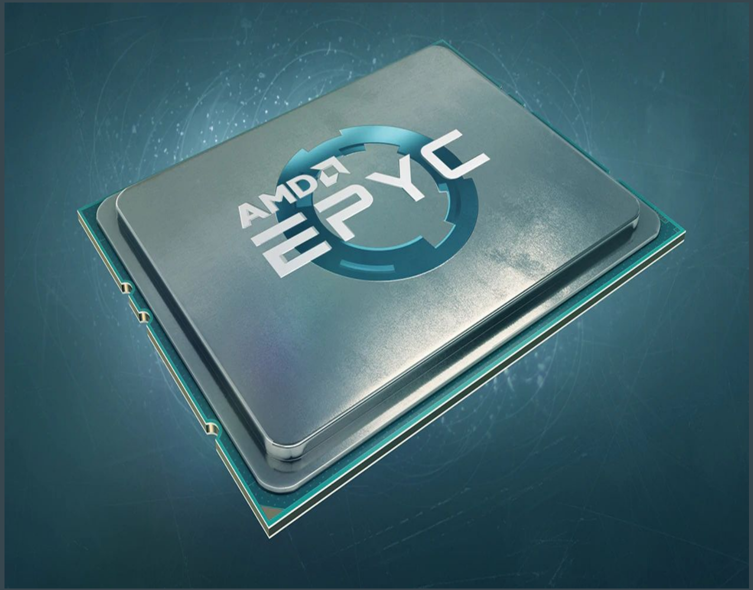
This method might be very slow because of space charge limitations. There will be more rapid methods. We could first make, perhaps by some photo process, a screen which has holes in it in the form of the letters. Then we would strike an arc behind the holes and draw metallic ions through the holes; then we could again use our sys-

MEMS Editor's Note: This manuscript addresses many current research issues. It is the transcript of a talk given by Richard P. Feynman on December 26, 1959, at the annual meeting of the American Physical Society at the California Institute of Technology, and was published as a chapter in the Reinhold Publishing Corporation book, *Miniaturization*, Horace D. Gilbert, Ed. It is reprinted with the consent of Van Nostrand Reinhold, New York, NY 10003.

The author, deceased, was with the California Institute of Technology, Pasadena, CA.

IEEE Log Number 9105621.





- First Intel computer chip : Intel 4004
- Consists of 2,300 transistors

- Current Zen microarchitecture : 32 core AMD Epyc
- Consists of 19,200,000,000 transistors (Nineteen billion)

Technology	No. of Transistors
Small Scale Integration (SSI)	Upto 100
Medium Scale Integration (MSI)	100 to 1000
Large Scale Integration (LSI)	1000 to 20K
Very large Scale Integration (VLSI)	20K to 10,00,000
Ultra Large Scale Integration (ULSI)	10,00,000 to 1,00,00,000

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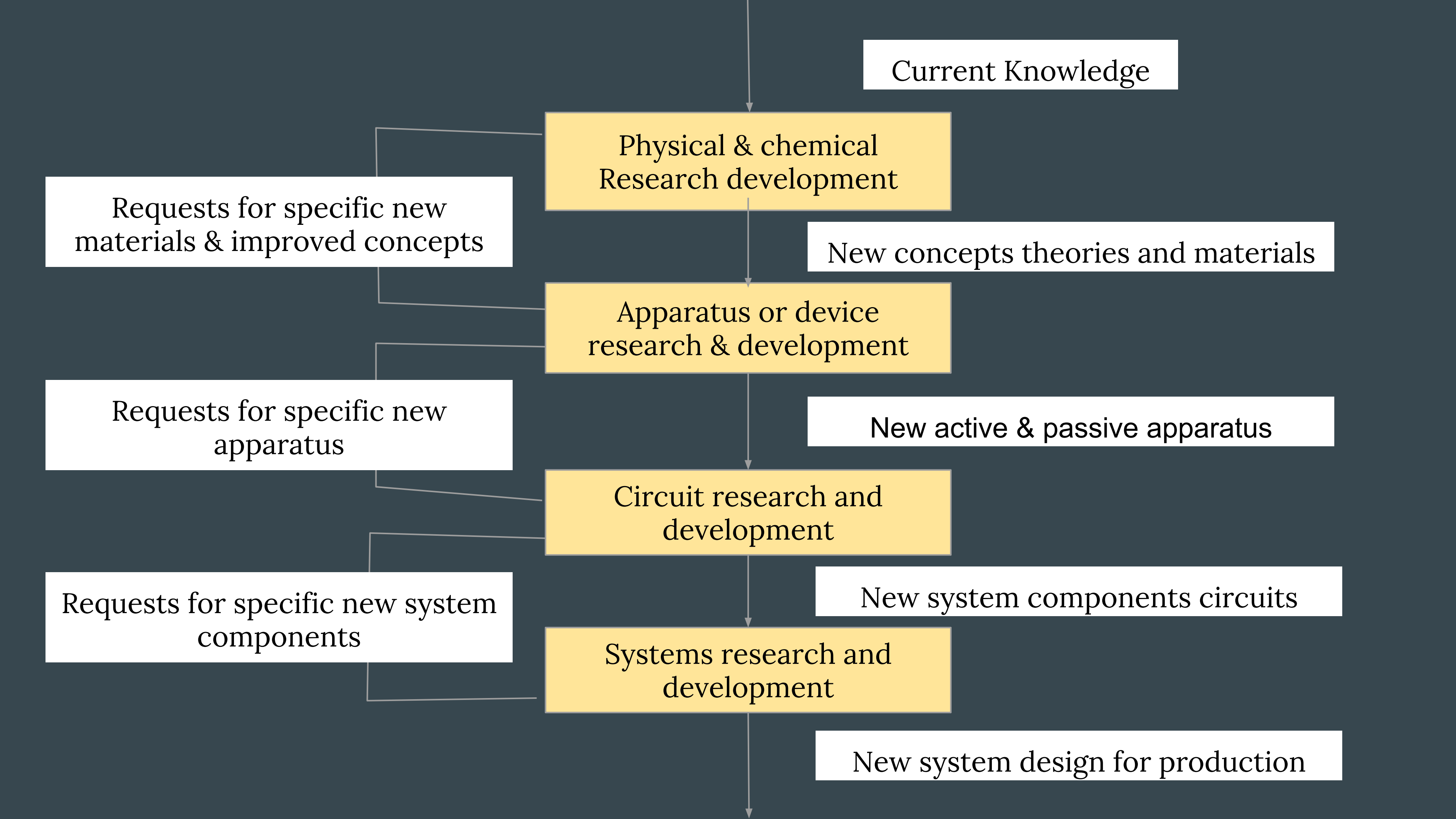
Sonotone 1010

….First commercial device to use the transistor.


Current Knowledge
Physical & chemical Research development
Requests for specific new materials & improved concepts
New concepts theories and materials
Apparatus or device research & development
Requests for specific new apparatus
New active & passive apparatus
Circuit research and development
Requests for specific new system components
New system components circuits
Systems research and development
New system design for production

Successive Ordinal Stages : -

1. **Zero-Order approximation** is the first attempt at a solution to achieve the overall goal.

- Zero order system stage
- Zero order circuit stage
- Zero order device stage
- Zero order chemical physical stage

2. **First-Order solution**

- New refinements & even new circuits may be indicated.Alternative circuits for a given function may be considered
- Meeting first order requirements with reasonable goals.

Phase I : *Formulation of the requirements of the characteristics of Transistor*

- Essential for a device engineer effect a compromise between what is optimally desired by the circuit engineer and what is achievable with good reproducibility, reliability and reasonable yields.

Phase II: *Analysis of Transistor Structures*

- By structure, I mean variables which can be nominally under the control of design & production engineers.

- Examples of structures : junction spacing. Resistivity,geometry and minority-carrier lifetime of a semiconductor

$$Z = Z(S1, S2, S3\ldots\ldots.Sn, b1, b2, b3\ldots\ldots\ldots bn)$$

Z represent open circuit impedance of transistor

Variables S_i represent all the structures

Variables b_i represent d-c biasing currents & voltages at which the device may be operated.

Outline

- npn Bipolar Junction Technology
- Modifications to the standard npn BJT technology

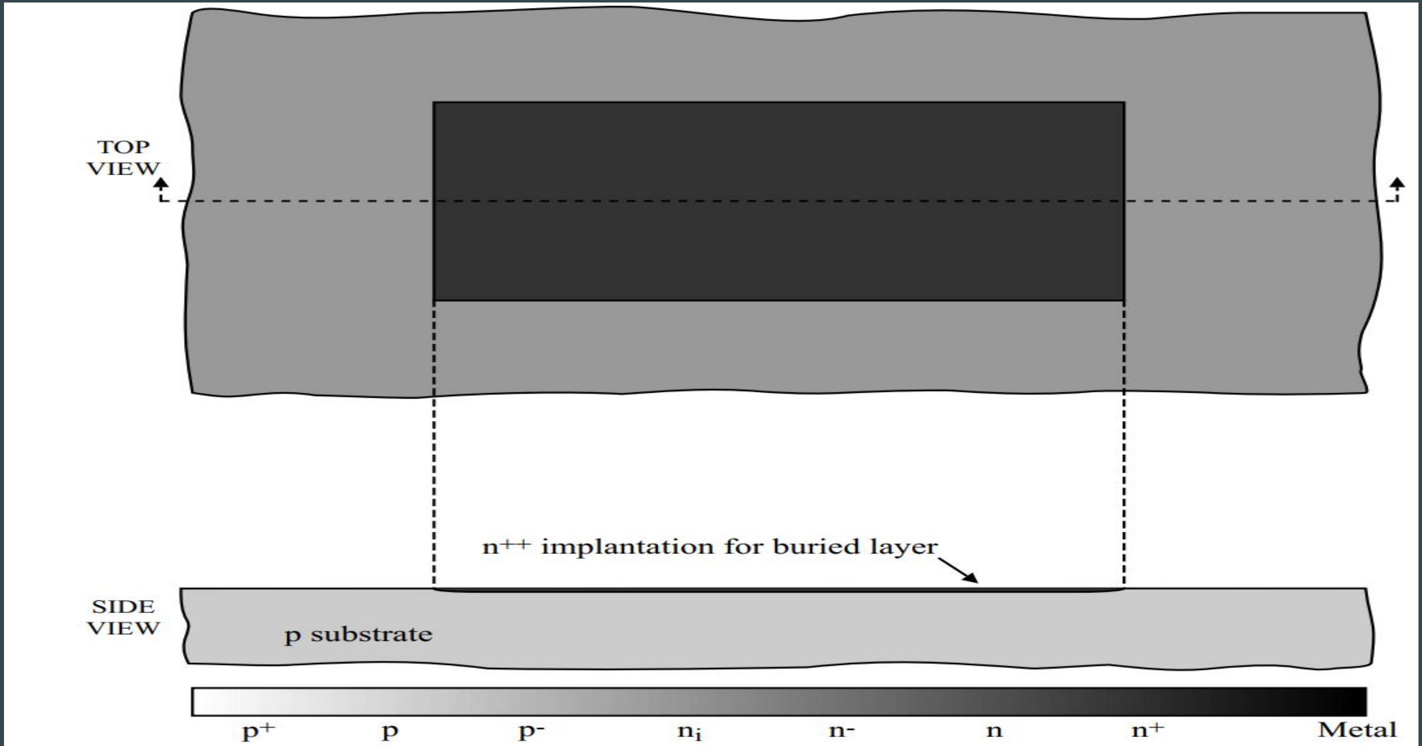
Major Processing Steps for a Junction Isolated BJT Technology

Start with a p substrate.

1. Implantation of the buried n+ layer
2. Growth of the epitaxial layer (MBE/MOCVD)
3. p+ isolation diffusion
4. Base p-type diffusion
5. Emitter n+ diffusion
6. p+ ohmic contact
7. Contact etching
8. Metal deposition and etching
9. Passivation and bond pad opening

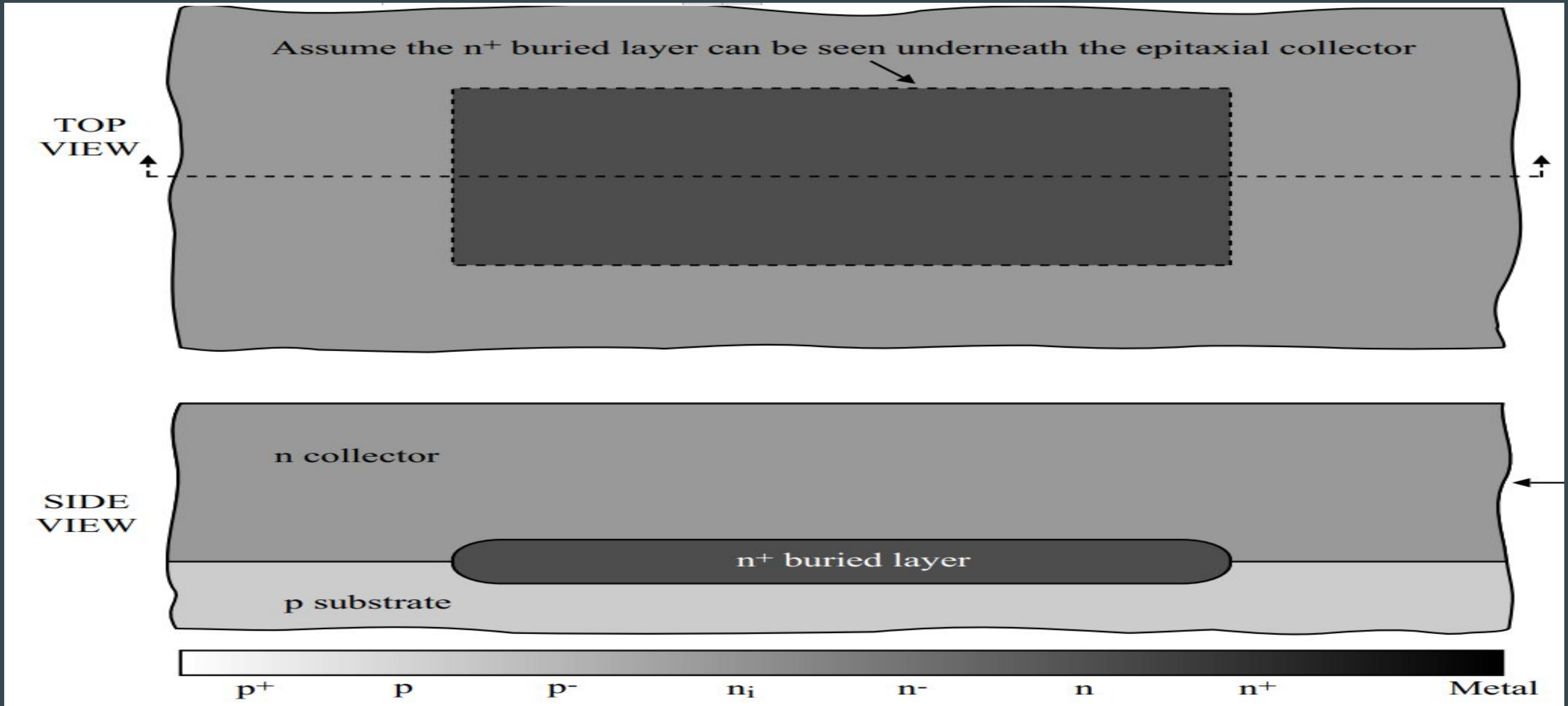
Implantation of the Buried Layer (Mask Step 1)

Objective: the buried layer is to reduce the collector resistance.



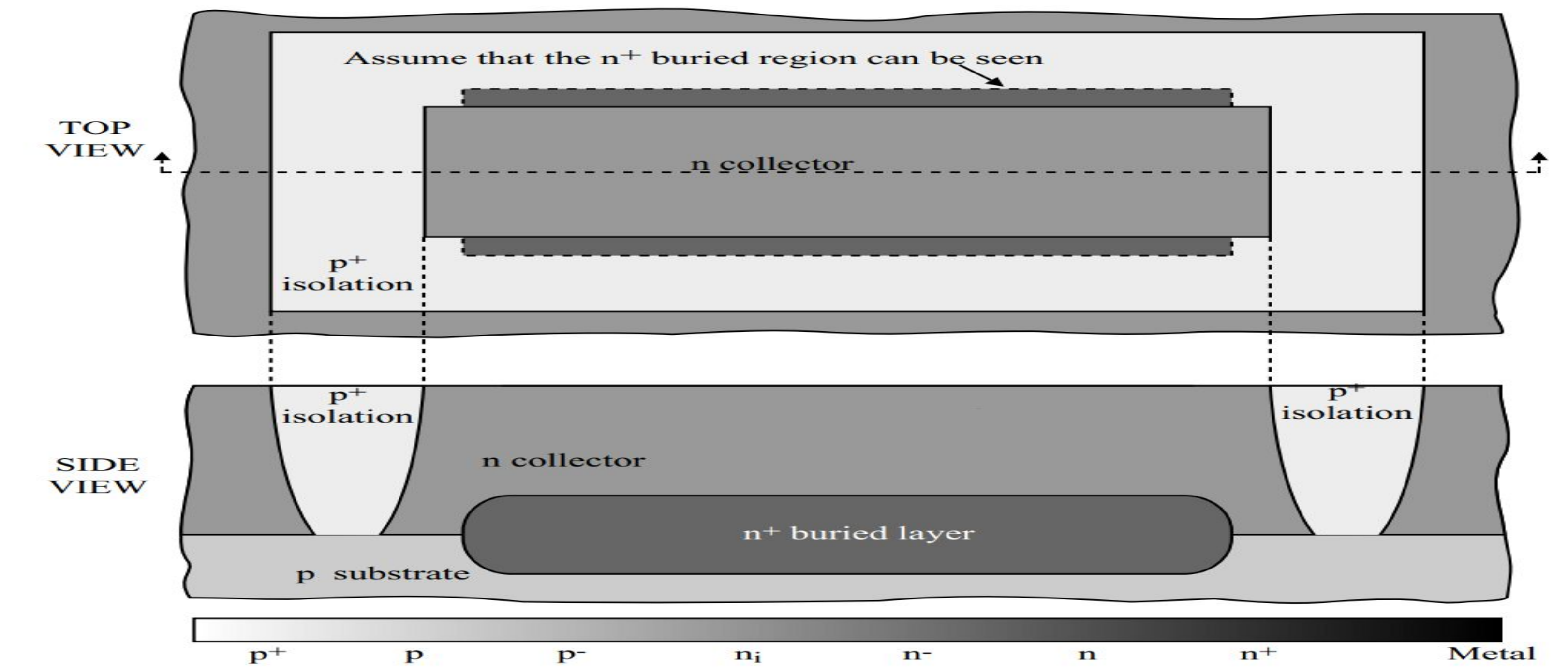
Epitaxial Layer (No Mask Required)

Objective: To provide the proper n-type doping in which to build the npn BJT



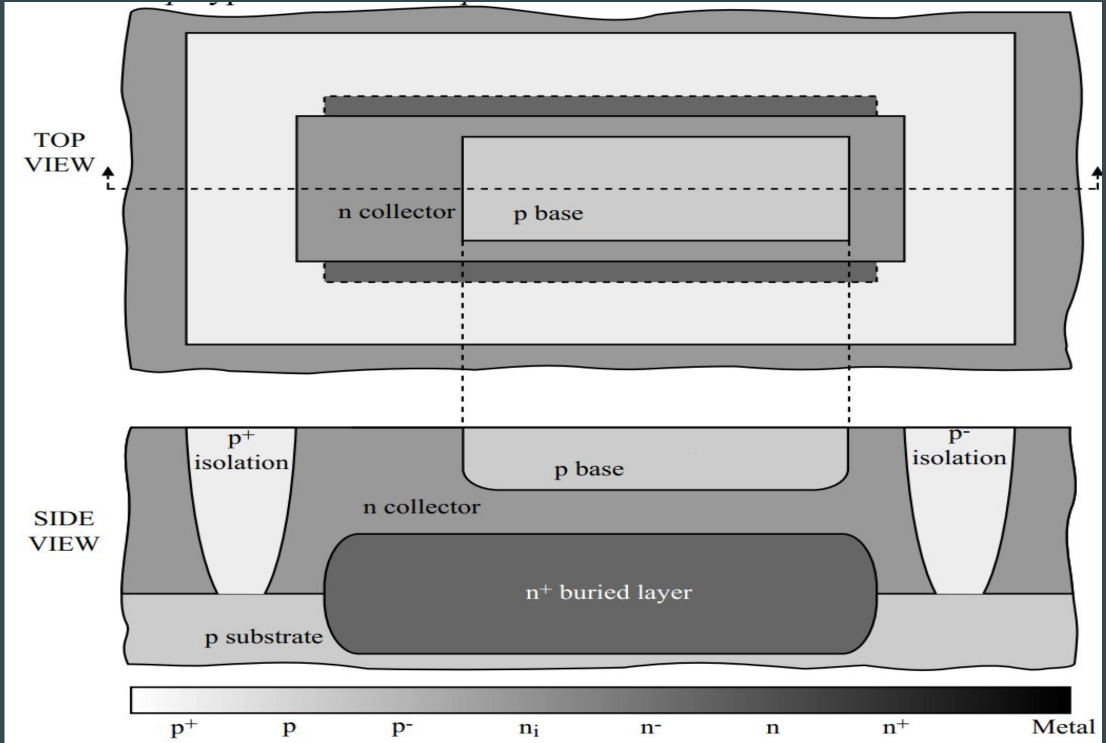
p+ isolation diffusion (Mask Step 2)

Objective: of this step is to surround (isolate) the npn BJT by a p+ diffusion. These regions also permit contact to the substrate from the surface



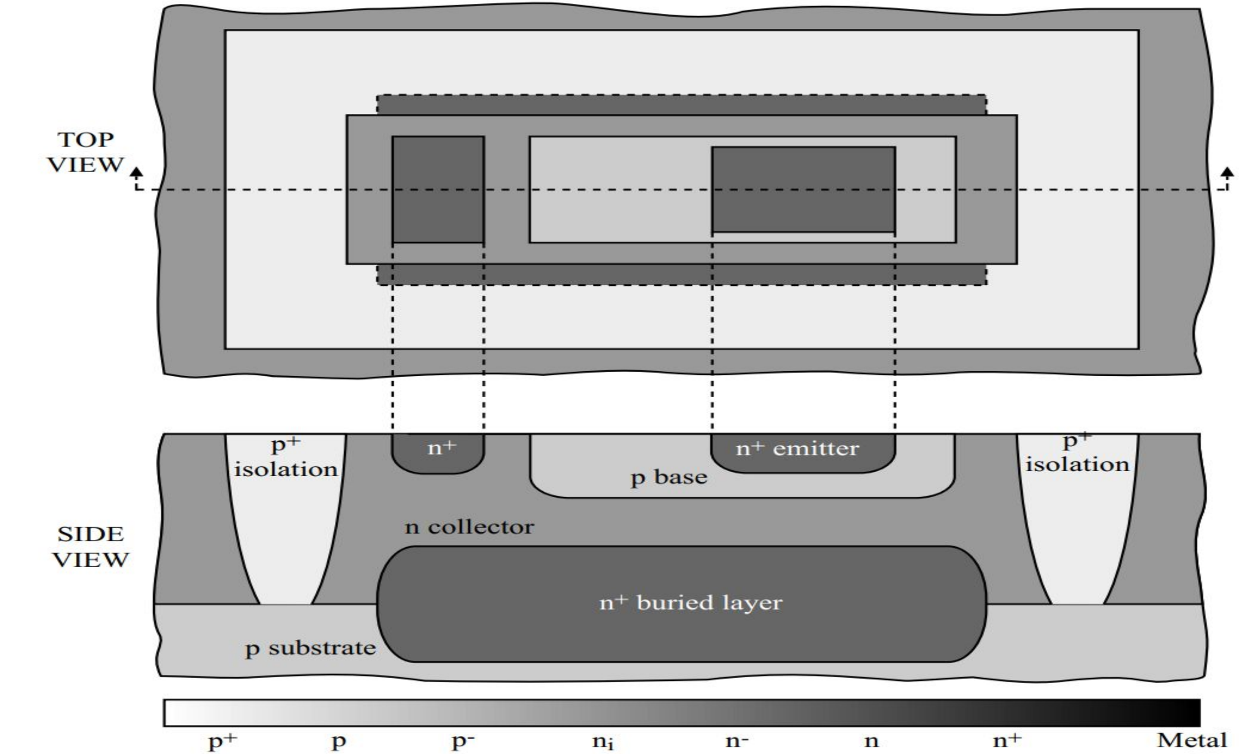
Base p-type diffusion (Mask Step 3)

The step provides the p-type base for the npn BJT



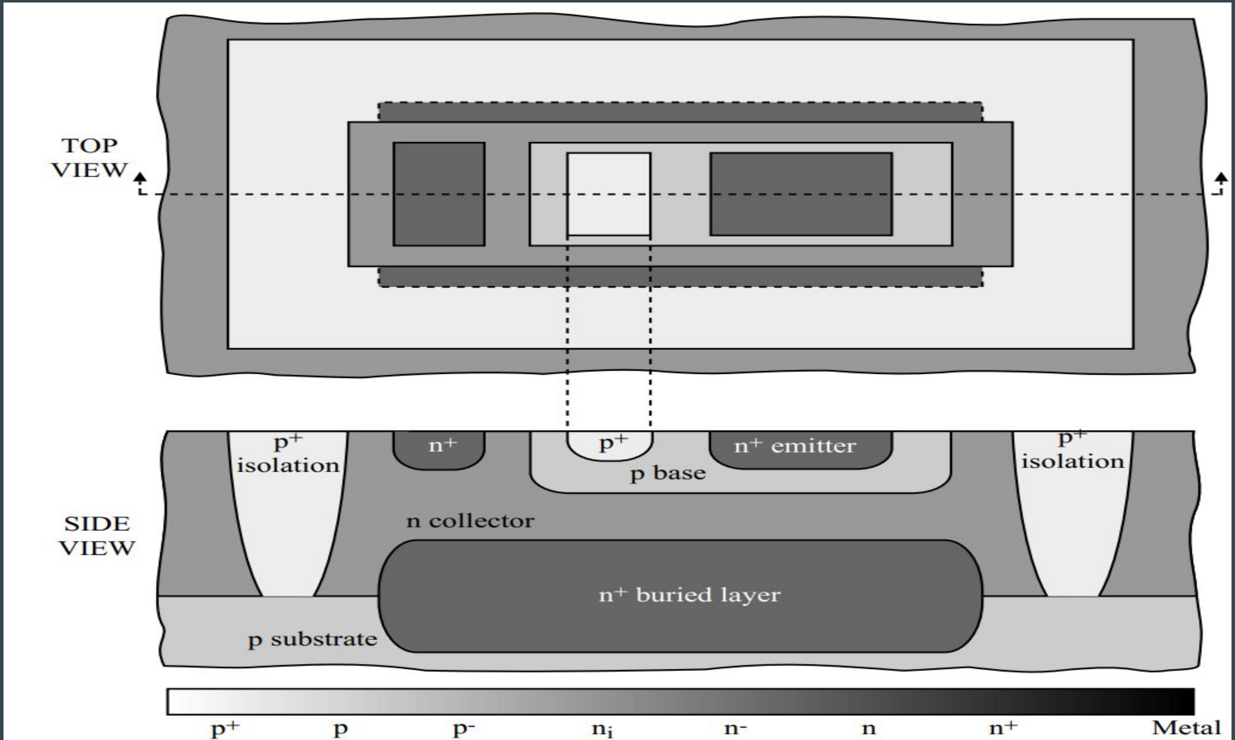
Emitter n+ diffusion (Mask Step 4)

This step implements the n+ emitter of the npn BJT and the ohmic contact to the collector



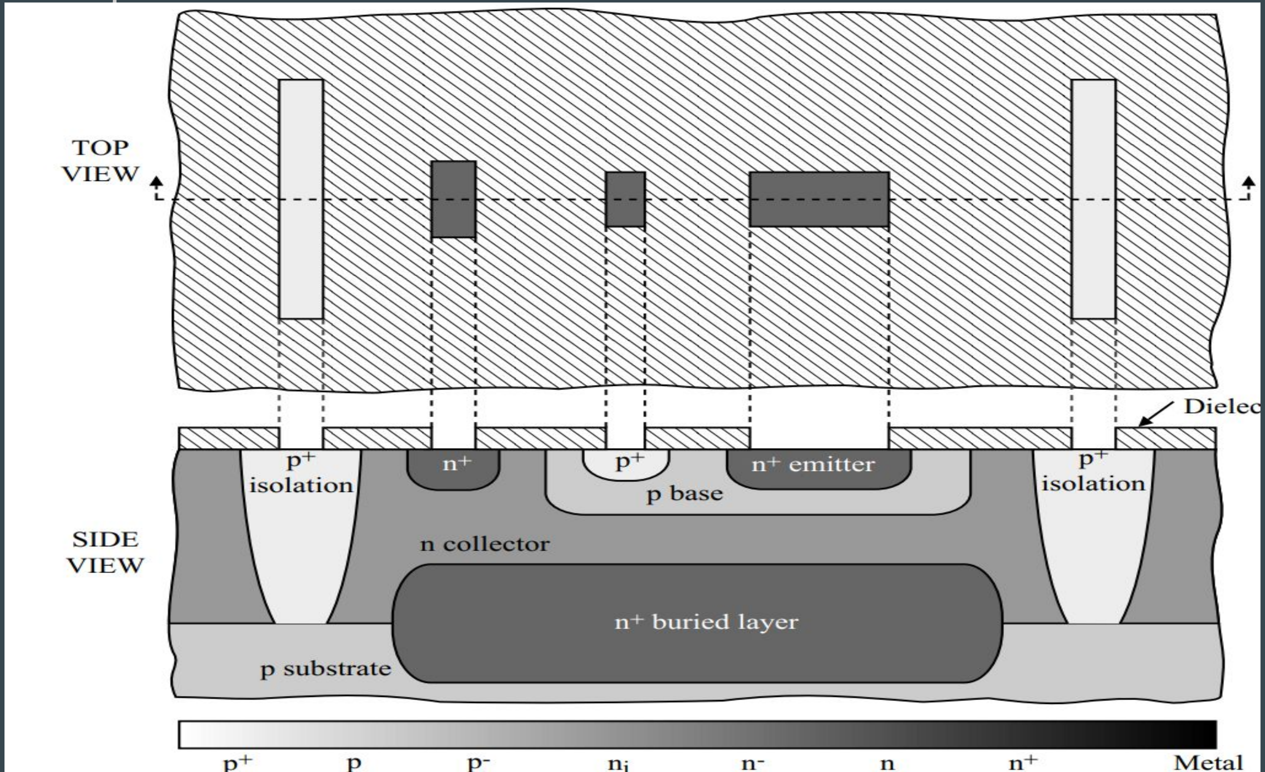
p+ ohmic contact (Mask Step 5)

This step permits ohmic contact to the base region if it is not doped sufficiently high



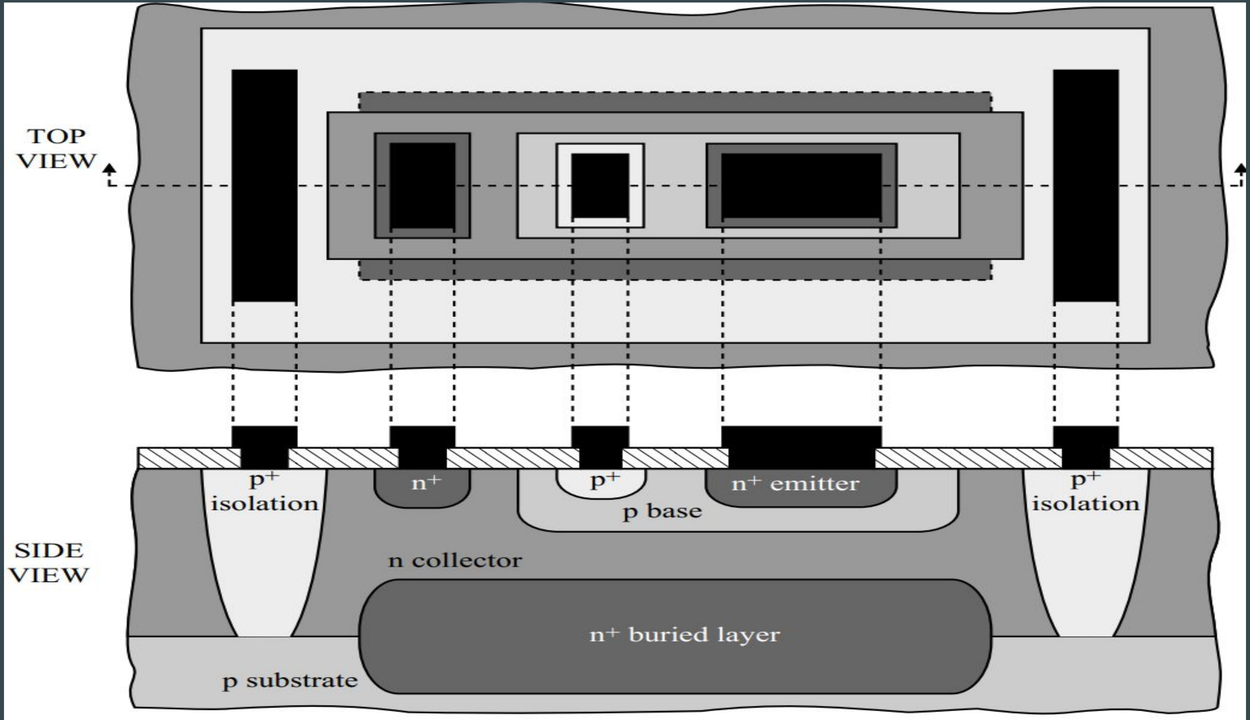
Contact etching (Mask Step 6)

This step opens up the areas in the dielectric area which metal will contact



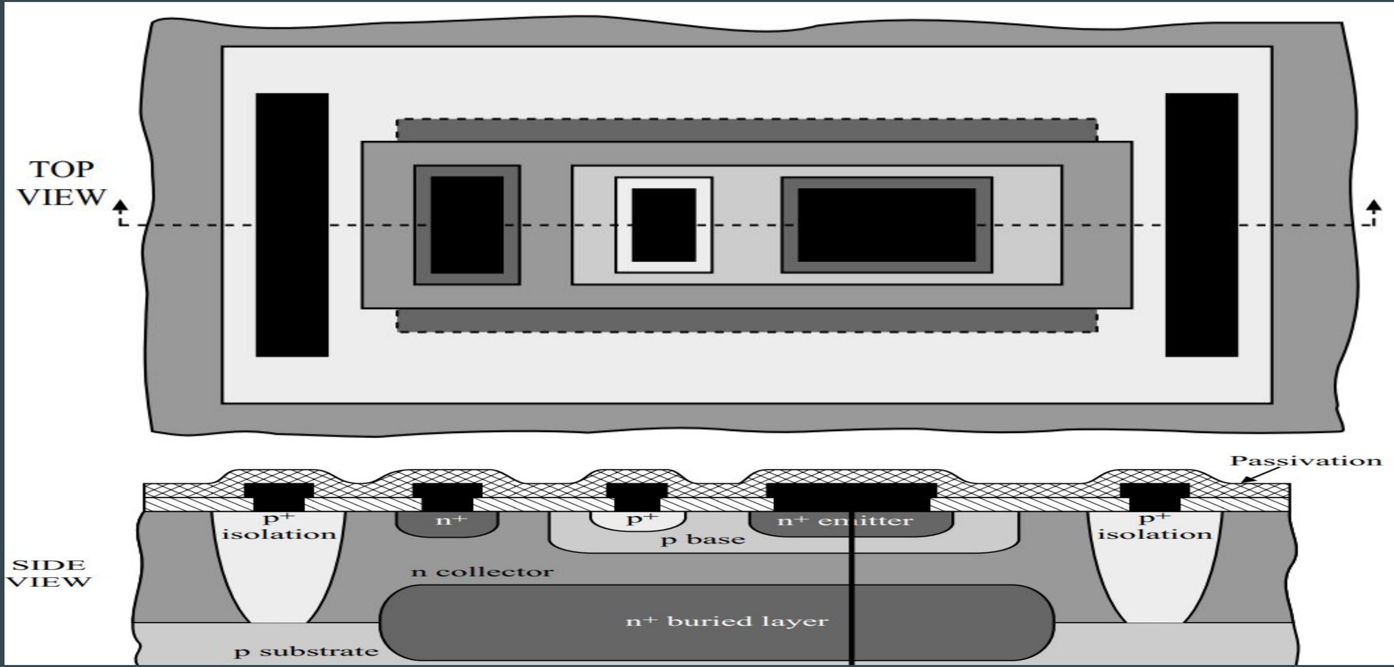
Metal deposition and etching (Mask Step 7)

In this step, the metal is deposited over the entire wafer and removed where it is not wanted.



Passivation (Mask Step 8)

Covering the entire wafer with glass and opening the area over bond pads (which requires another mask)



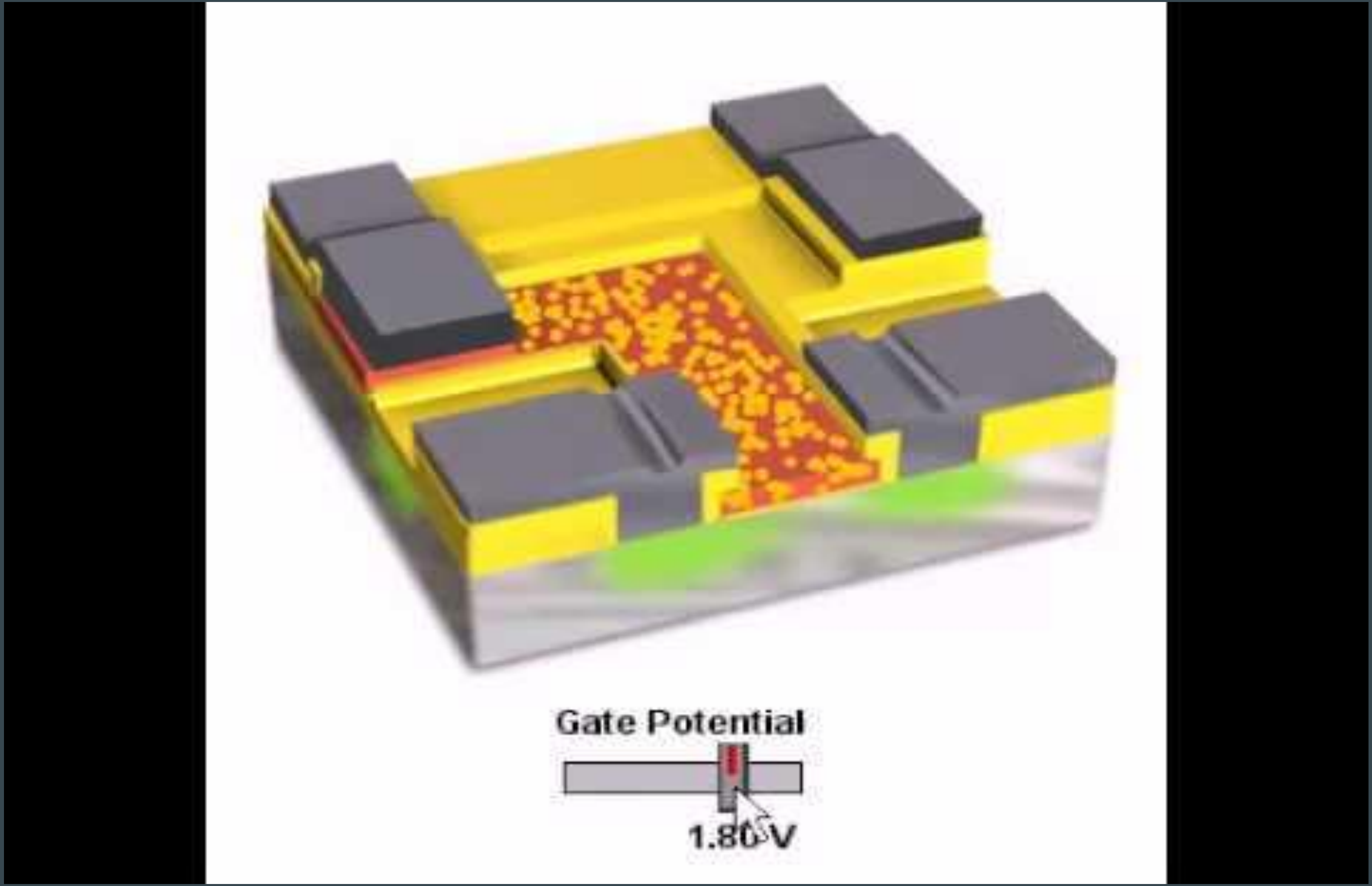
Stochastic Processes

Advances by

Prof. Udayan Ganguly, EE dept, IITB: Strategic Semiconductors

Prof. Punit Parmananda, Physics dept, IITB : regular patterns by pitting corrosion

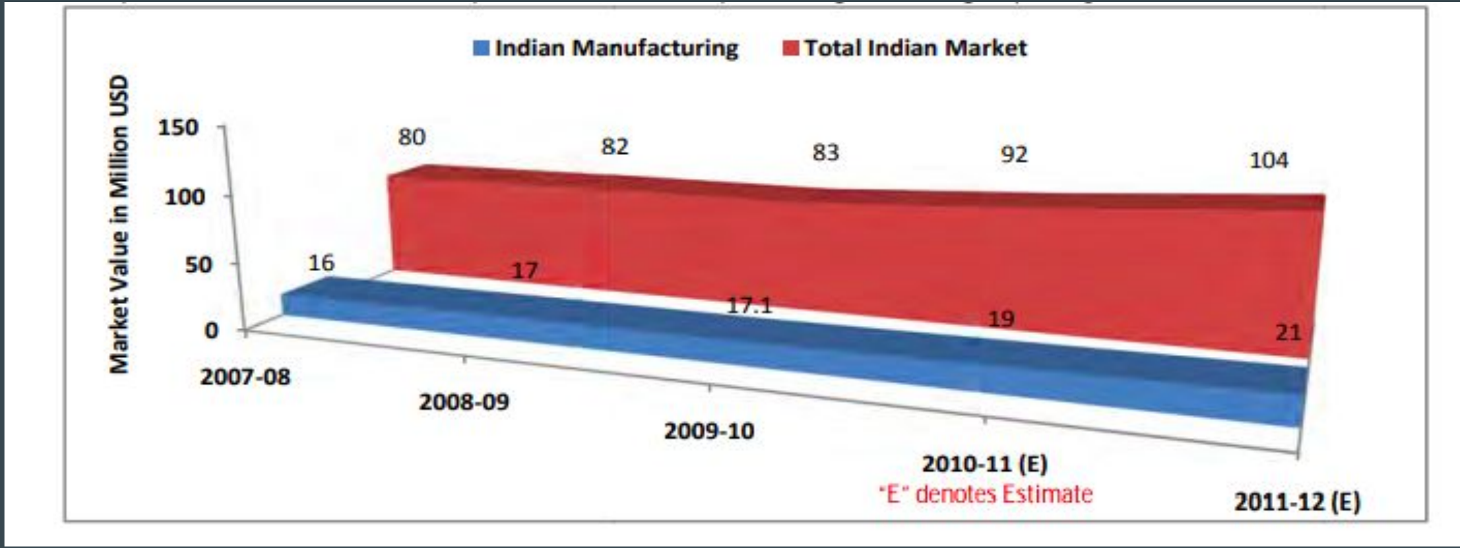
Fabrication Animation



Indian Transistor market

Sl. No.	Heads	Description
1	Overall Indian Market Size in FY 2009-10	USD 83 Million
2	Ratio of Imports: Indian Manufacturing in FY 2009-10	80:20
3	Growth in FY 2009-10	1%
4	Export in FY 2009-10	USD 3 Million
5	Market Size by type of Transistor	Bipolar Junction Transistor (BJT), Field Effect Transistor (FET), Metal Oxide Field Effect Transistor (MOSFET), Insulated Gate Bipolar Transistor (IGBT)
6	Key Application Segments	Consumer durables & Lighting
7	Estimated Growth in FY 2010-11	12%
8	Estimated Ratio of Imports : Indian Manufacturing in FY 2010-11	70:30

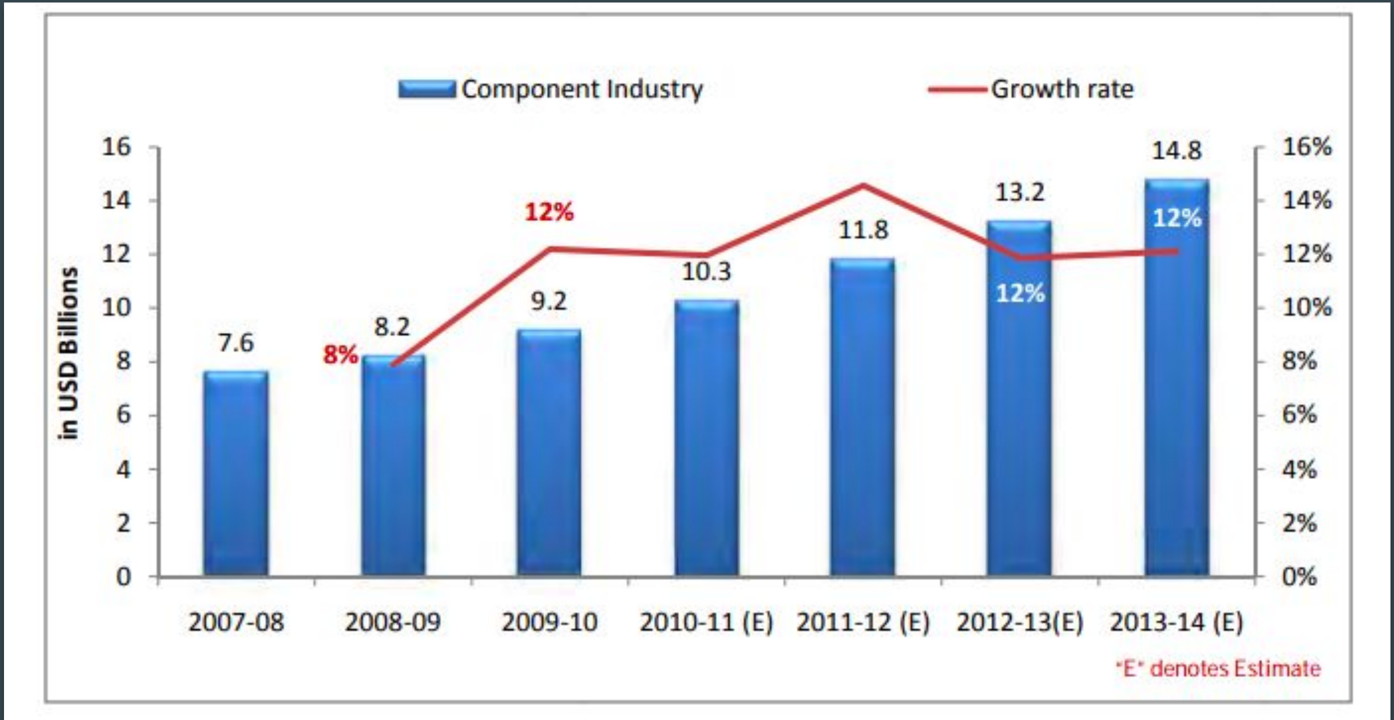
Current and Past Trends



The overall market size for transistors in India is estimated at USD 83 million for the FY 2009- 10 with imports accounting for 80 % of the total market. The transistors are largely imported from China & Taiwan. In addition, a considerable proportion of transistors used in automotive and power electronics are imported from Europe owing to its high quality

Major electronic hubs in India

Growth of Indian Electronics components market



Global Analysis

- India's electronics market is one of the largest in the world in terms of consumption, is predicted to grow to approximately US$400 billion by 2020 from $69.6 billion in 2012

- Report of the NITI Aayog, electronics industry's contribution to GDP is only 1.7% in India, compared to 15.5% in Taiwan, 15.1% in South Korea and 12.7% in China.

Salient Aspects of Indian Transistor Industry

- Continental Devices India Limited and Bharat Electronics limited are the two leading manufacturers of transistors in India
- The Indian transistor market is estimated to grow at a CAGR of 11% for the next 3 years and the market size in FY2011-12 is expected to reach USD 104 Million
- Growing demand in the automotive and consumer durable market are the two key factors that is expected to drive the transistor industry, thus positively affecting its growth rate.
- Non Availability of raw materials like molding compound, silicone wafer, lead frames etc., high import duties on raw material and competitive component pricing from players in China are cited as the key restraints for the transistor manufacturing industry in India

Developments and Improvements

Single transistor 7 nm scale devices were first produced by researchers in the early 2000s.

In 2002, IBM produced a 6 nm transistor.

In 2003, NEC produced a 5 nm transistor.

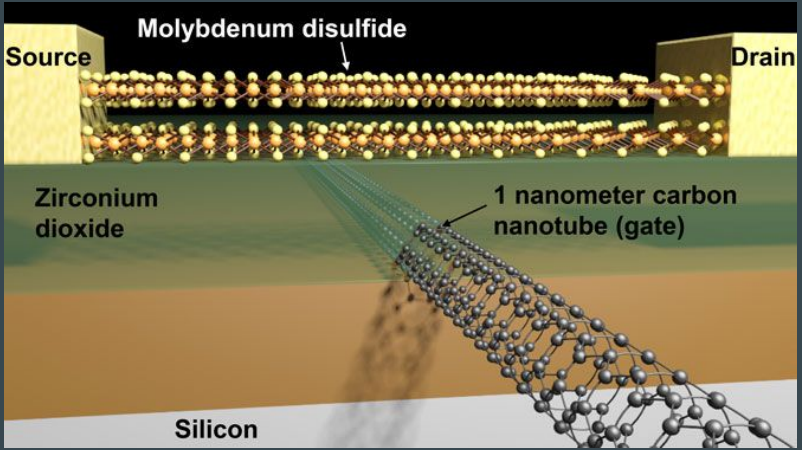
In 2015, IMEC and Cadence had fabricated 5 nm test chips. The fabricated test chips are not fully functional devices but rather are to evaluate patterning of interconnect layers.

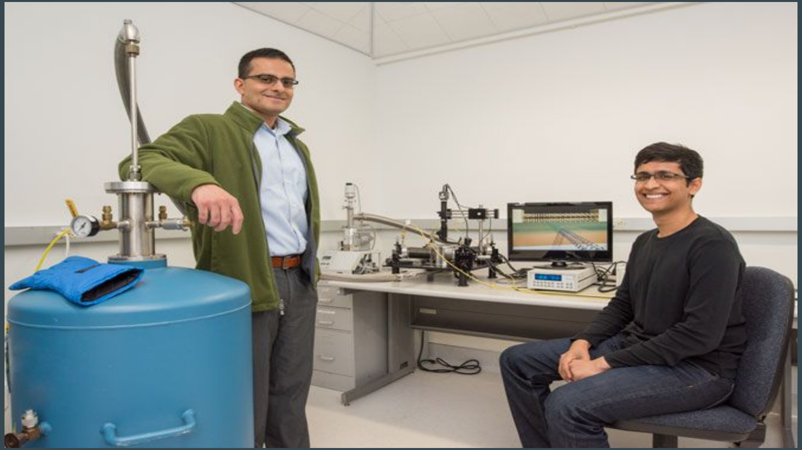
In 2015, Intel described a lateral nanowire (or gate-all-around) FET concept for the 5-nm node.

In 2017, IBM revealed that they had created 5 nm silicon chips, using silicon nanosheets in a gate-all-around configuration (GAAFET), a break from the usual FinFET design.

Research Improvements

In 2016, researchers at Berkeley Lab created a transistor with a working 1-nanometer gate. The field-effect transistor utilized MoS_2 as the channel material, while a carbon nanotube was used to invert the channel. The effective channel length is approximately 1 nm. However, the drain to source pitch was much bigger, with micrometre size.





References

https://en.wikipedia.org/wiki/Electronics_and_semiconductor_manufacturing_industry_in_India

http://meity.gov.in/writereaddata/files/ELCOMOS_Report_23412.pdf

https://www.electrical4u.com/transistor-manufacturing-techniques/

https://www.tutorialspoint.com/vlsi_design/vlsi_design_digital_system.htm

Neurotechnology Group, Berlin Institute of Technology, IEEE Xplore Digital Library. "Regression Methods for Virtual Metrology of Layer Thickness in Chemical Vapor Deposition." January 17, 2014. Retrieved November 9, 2015.

"8 Things You Should Know About Water & Semiconductors | China Water Risk". chinawaterrisk.org. Retrieved 2017-09-10.

"Top 10 Worldwide Semiconductor Sales Leaders - Q1 2017 - AnySilicon". AnySilicon. 2017-05-09. Retrieved 2017-11-19.

"A Survey Of Architectural Techniques for Managing Process Variation", ACM Computing Surveys, 2015

"Introduction to Semiconductor Technology" (PDF). p. 6. |first1= missing |last1= in Authors list (help)

"Wafer Backgrind".

CNET. "Why tech pollution's going global." April 25, 2002. Retrieved November 9, 2015.

Questions